Heterogeneous Integration, An Approach to High Density and High Flexibility Electronic Packaging. S. A. D'Agostino, D. Schatzel, Jet Propulsion Laboratory, 4800 Oak Grove Drive MS 83-204, Pasadena, CA 91109, saverio@jpl.nasa.gov.

Introduction: Key to the design of spacecraft for exploration of the outer planets will be the development of highly integrated and mass/volume efficient electronic systems. Integration must be developed in two major aspects. The electronic packaging approach must be capable of interconnecting various components at a scale comparable with that on the components themselves (chip scale) and it must facilitate efficient integration of the electronics with elements of the spacecraft such as structure or antennae. The concept of "Heterogeneous Integration" is being explored in the "System On A Chip (SOAC) Project at JPL. The goal, of this approach to electronic packaging, is to enable the fabrication and assembly of complete electronic subsystems from components fabricated by a range of processes. Included in such a system could be MEMS sensors, SOI mixed signal ASICs, micro scale passive components and micro power systems, Fig.-1. Secondarily the compact size will enable distributed architectures and integrated assemblies.

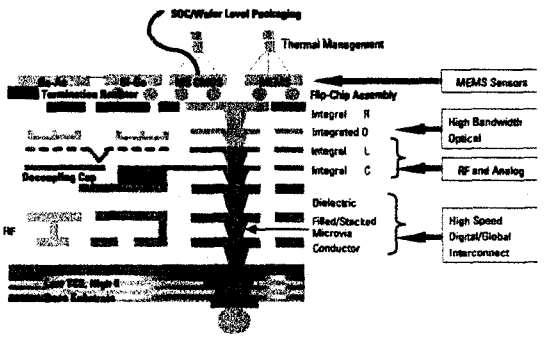

Figure-1. Concept of heterogeneous integration

Approach: There are several areas of technology development that are to be explored in bringing about the heterogeneous integration concept. The base-line technology is to incorporate "bump attachment" between the various components and the substrate. When possible this will entail wafer bumping prior to dicing and attachment. However, it is often the case with the stringent requirements of spacecraft electronics components will not be available as wafers and thus "single-point bumping" technologies will be a major area of development and validation testing. With the aim of enhancing long term reliability and to facilitate the adaptation of well understood processes the substrate for the integrated assembly is silicon. Another area of research involves the study of thin film eutectic bonding for attachment of components to substrate and assembling MEMS integral hermetic packages. Prof. Chin C. Lee is pursuing this work at The University of California at Irvine through the System On A Chip Project.

Architecture Considerations: The development of effective heterogeneous integration technology enables the efficient incorporation of distributed architectures for spacecraft electronics systems and enhances the applicability of primary busses for power and data transmission. The approach of the "nano-avionics node" (under development in SOAC) utilizes an assembly containing digital control and communication, mixed signal capability and power control integrated at the chip scale. Distributed sensor nodes would be particularly advantageous for monitoring the "health" of a spacecraft. "Health monitoring" becomes particularly critical for long missions and where autonomous operation and fault tolerance/correction is required.

Also enabled by the combination of heterogeneous integration and distributed architectures is the development of a whole new class of instruments utilizing arrays of MEMS or electronic sensors. Each sensor node has its own signal processing, communication and power electronics.

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